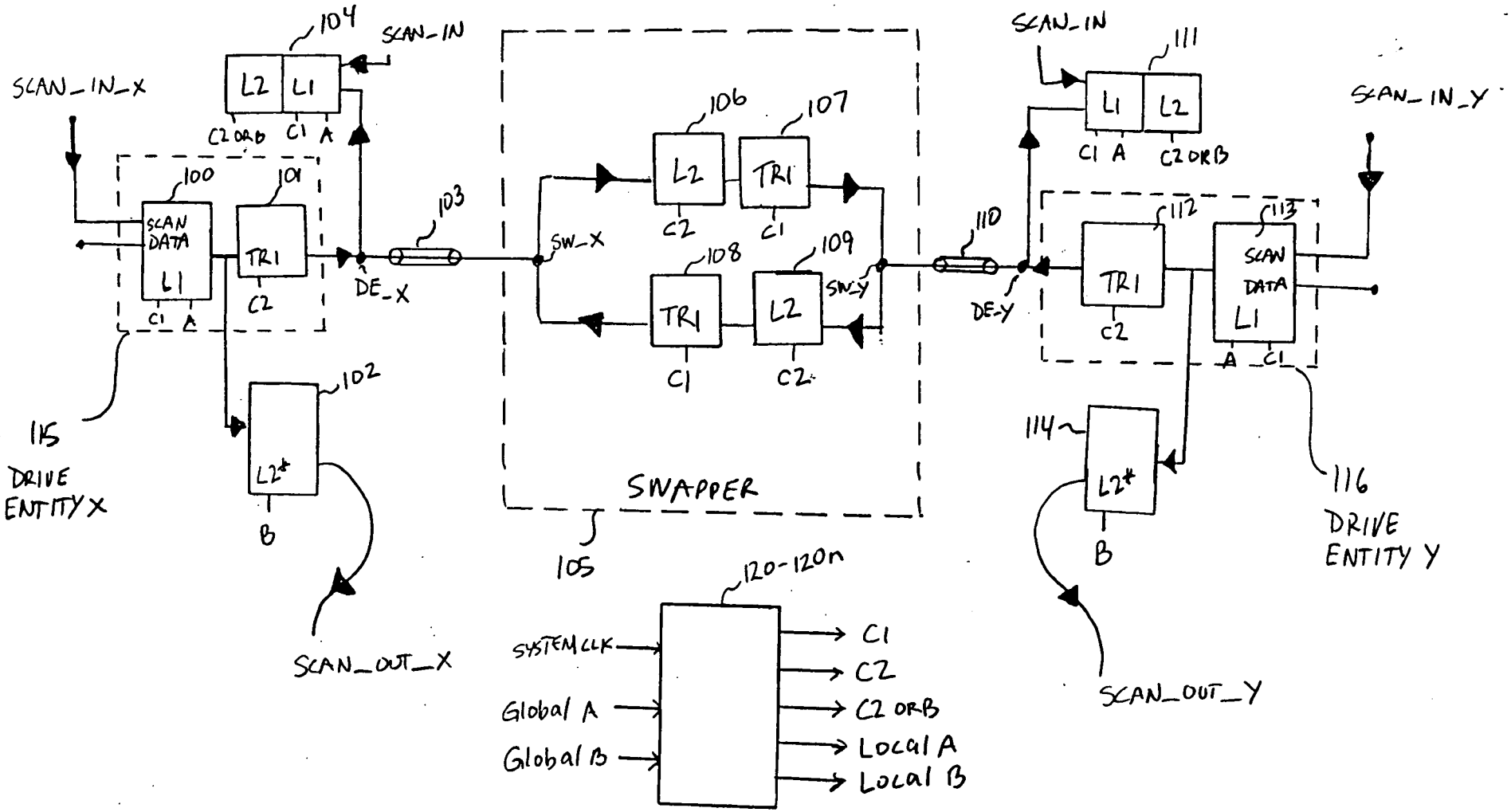


FIG. 1A

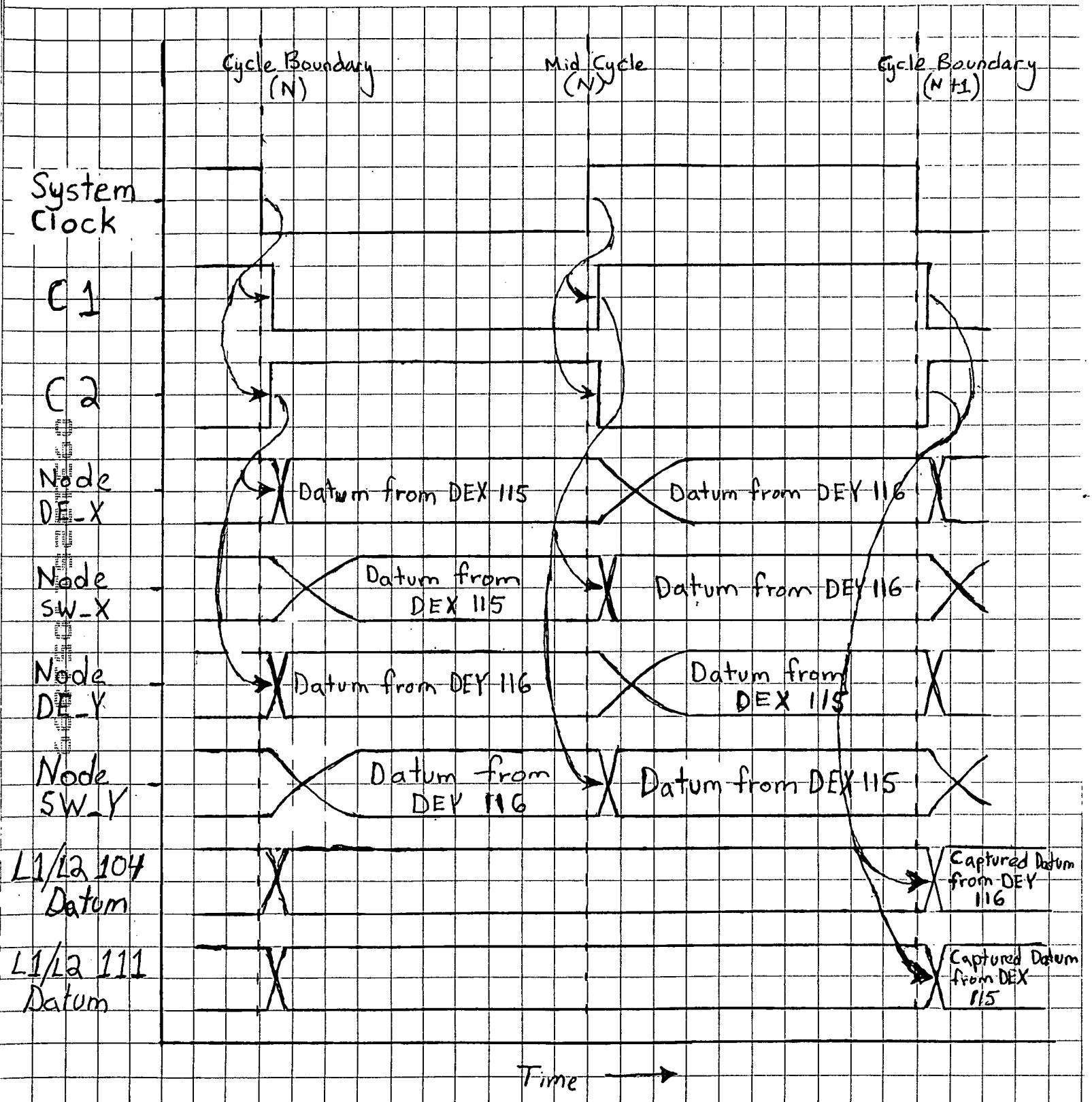


Figure 1B

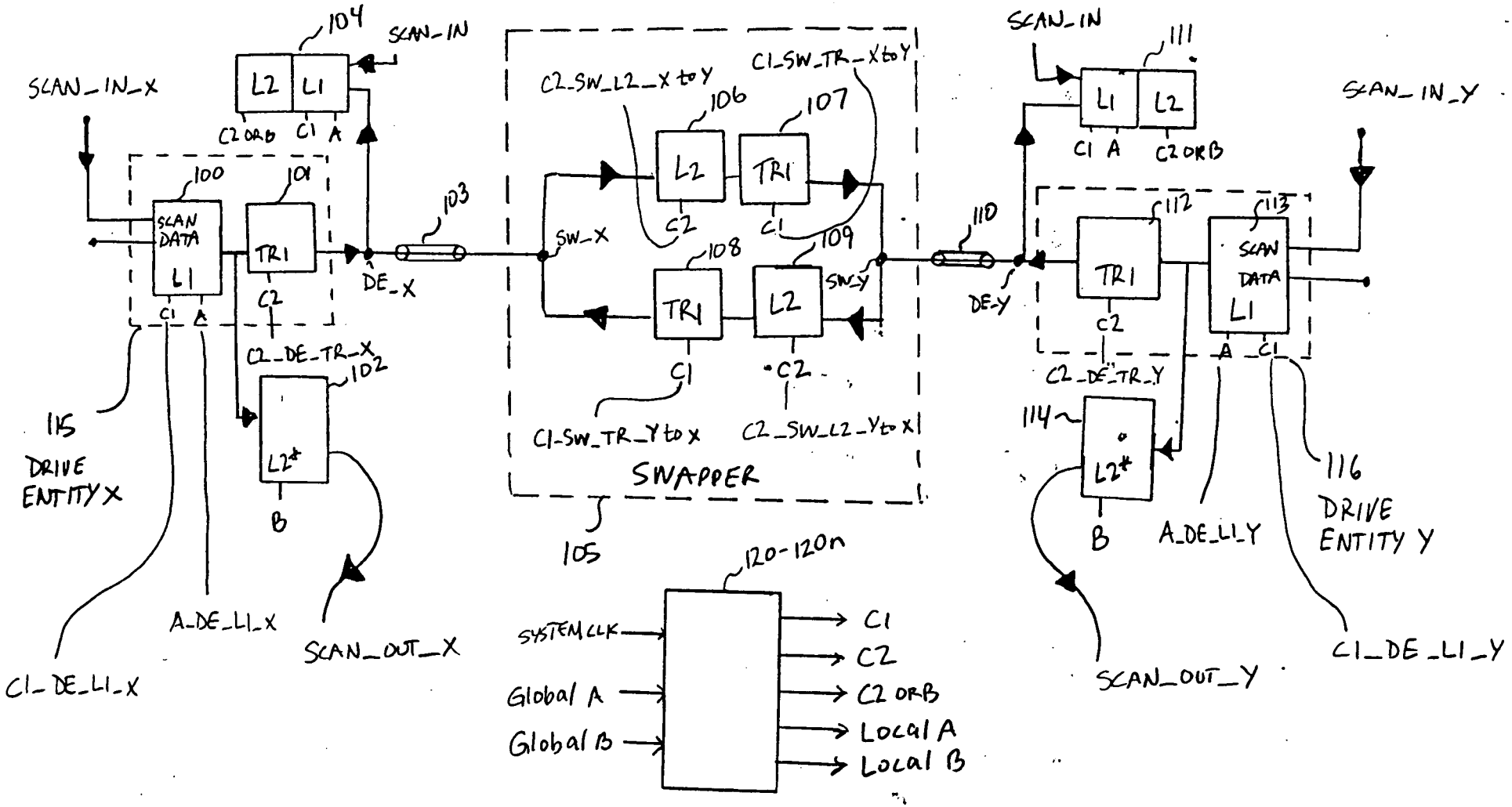


FIG. 1C

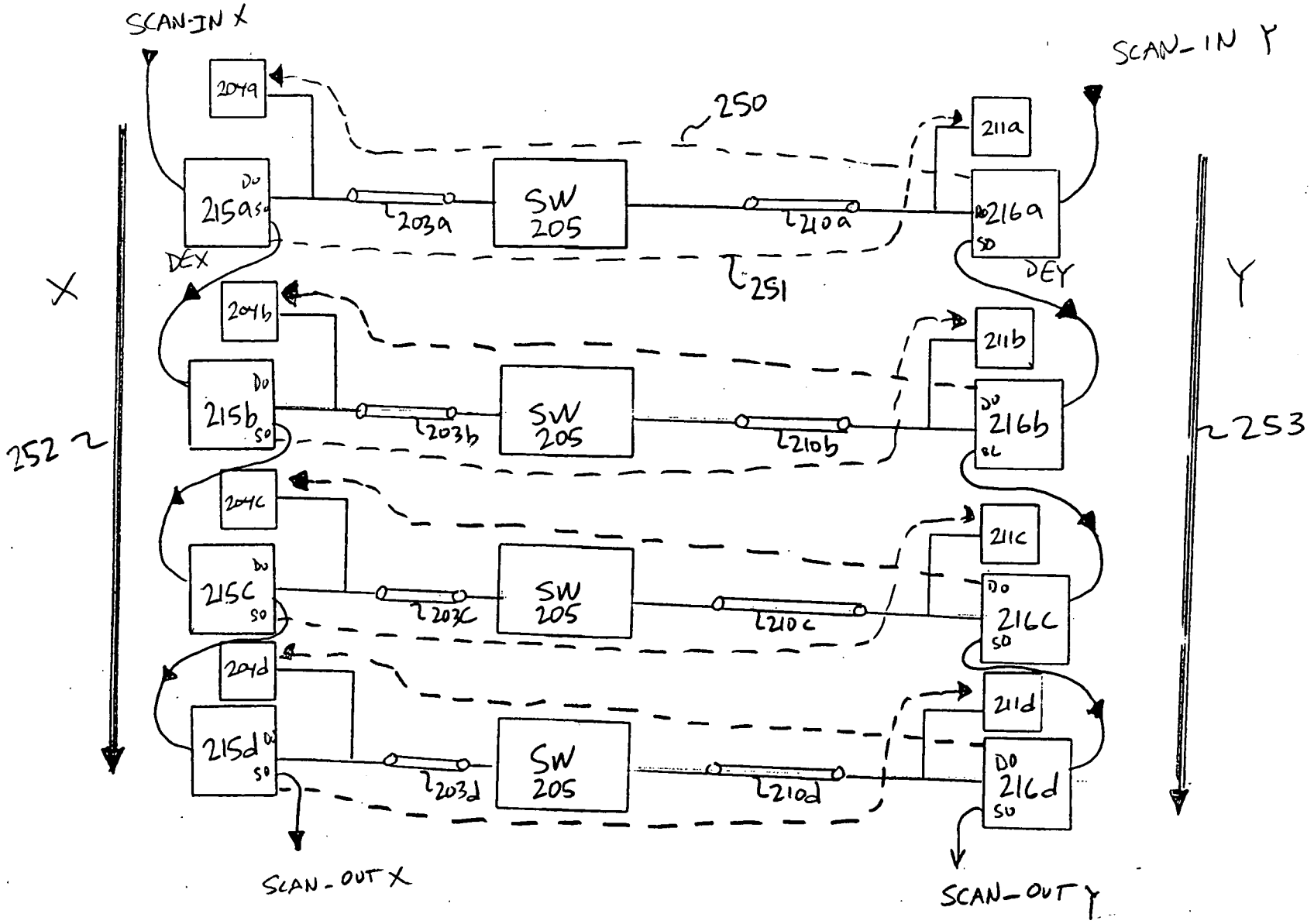


FIG 2A

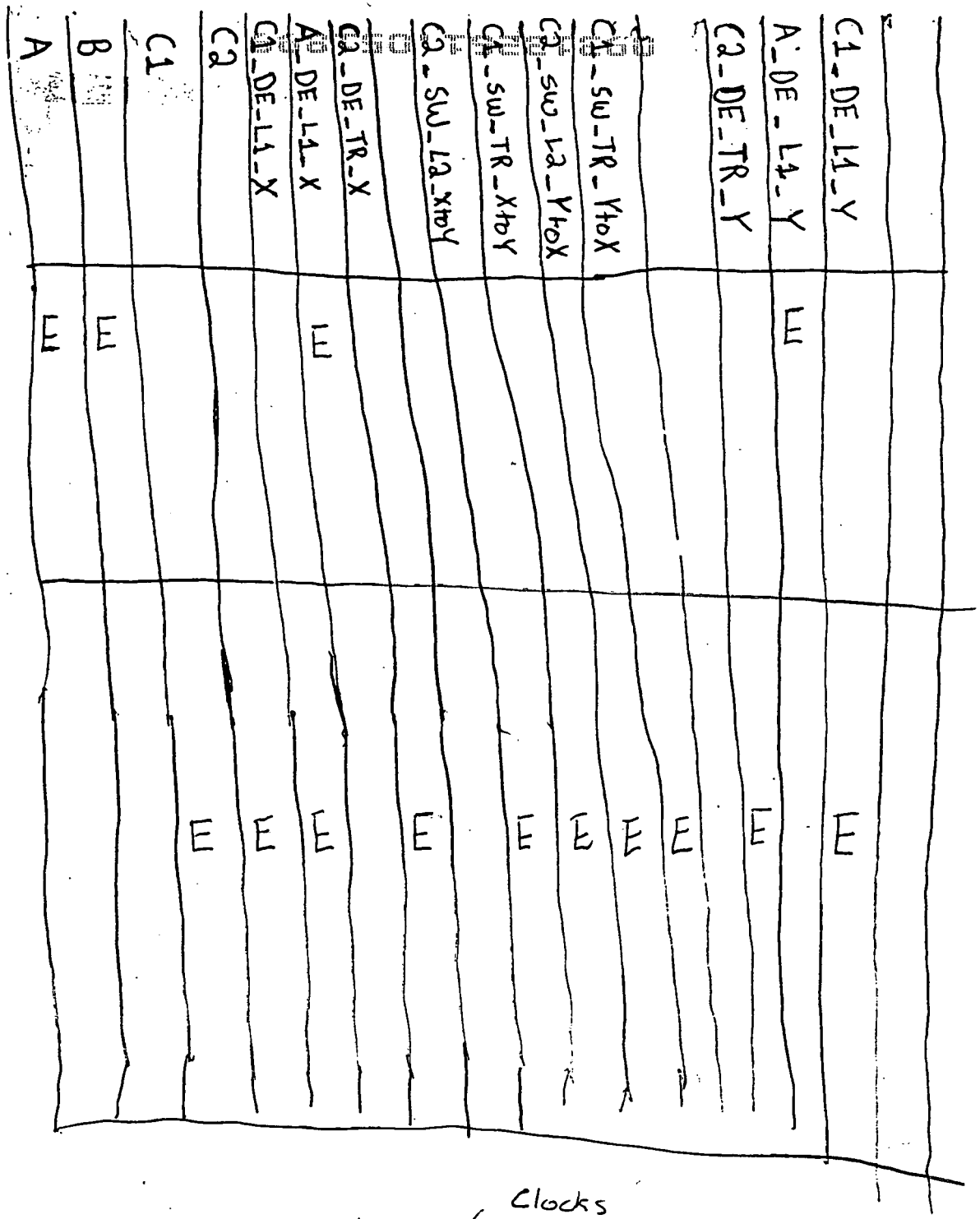


Figure 2B

E = Enabled

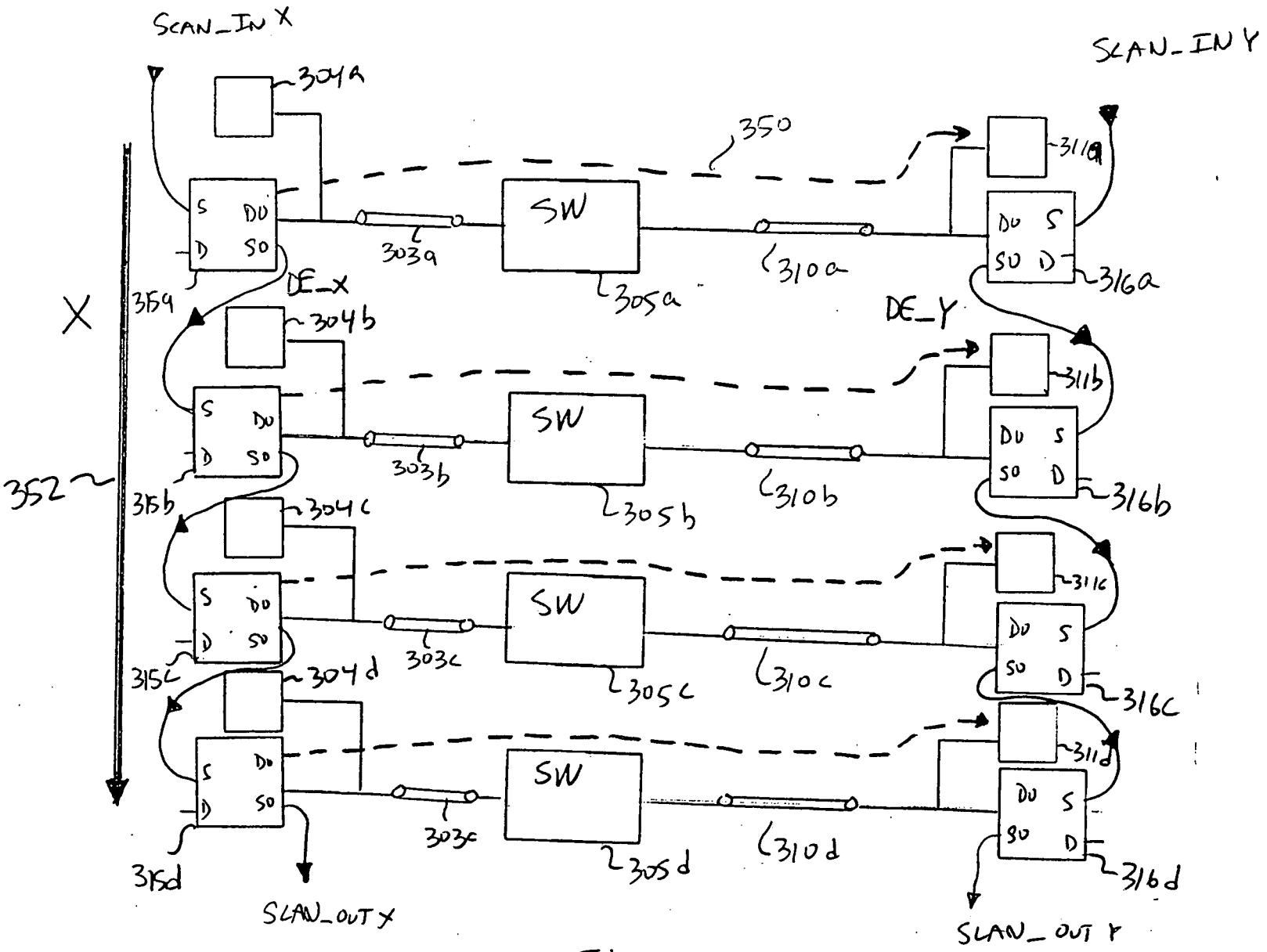

SCAN_IN X
SCAN_IN Y
304a
350
311a
S
DO
D
SO
303a
SW
310a
305a
316a
DE_X
DE_Y
315a
X
304b
311b
303b
310b
305b
316b
352
315b
304c
311c
303c
310c
305c
316c
315c
304d
311d
303c
310d
305d
316d
315d
SCAN_OUT X
SCAN_OUT Y

FIG 3A

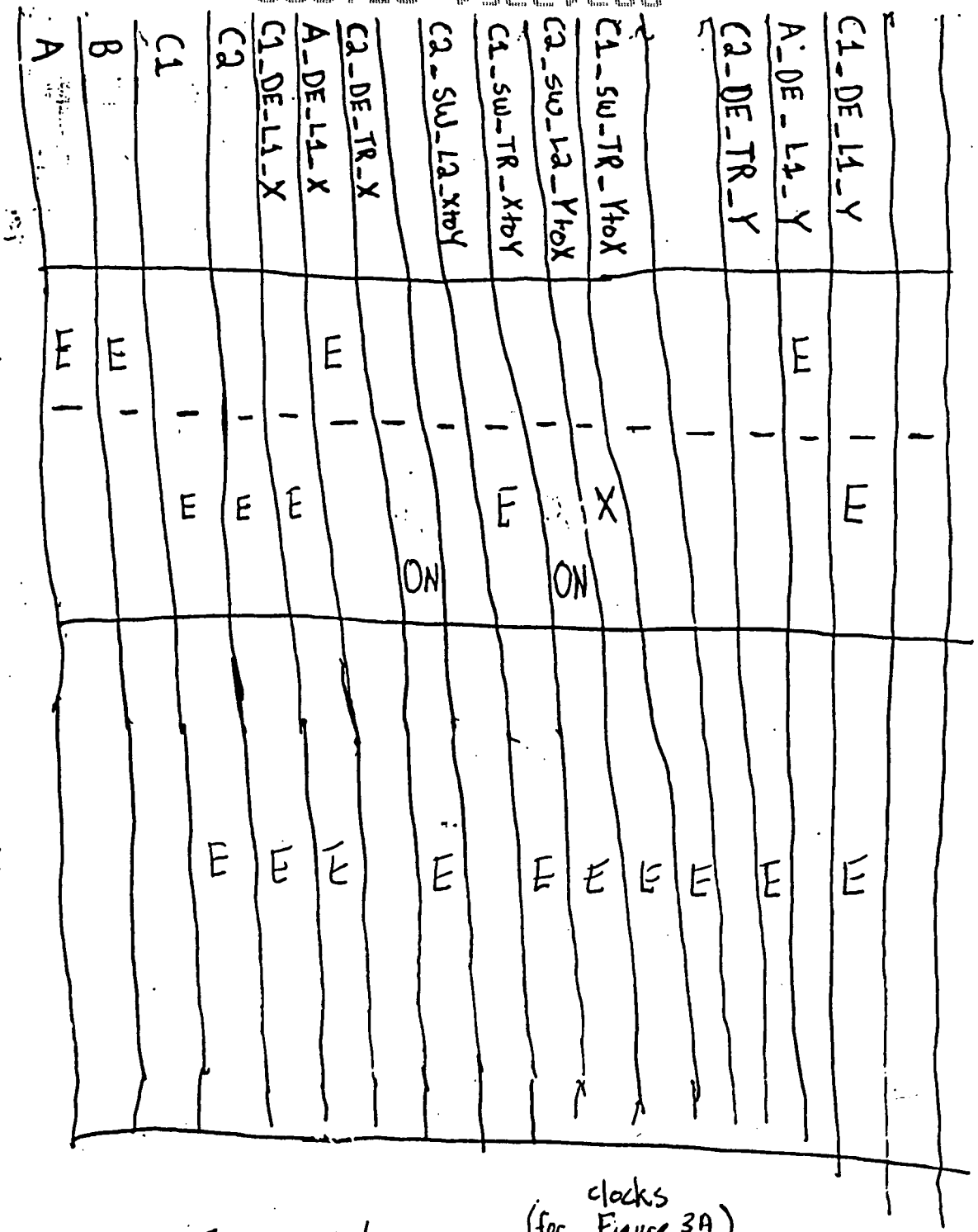


Figure 3B

E = Enabled

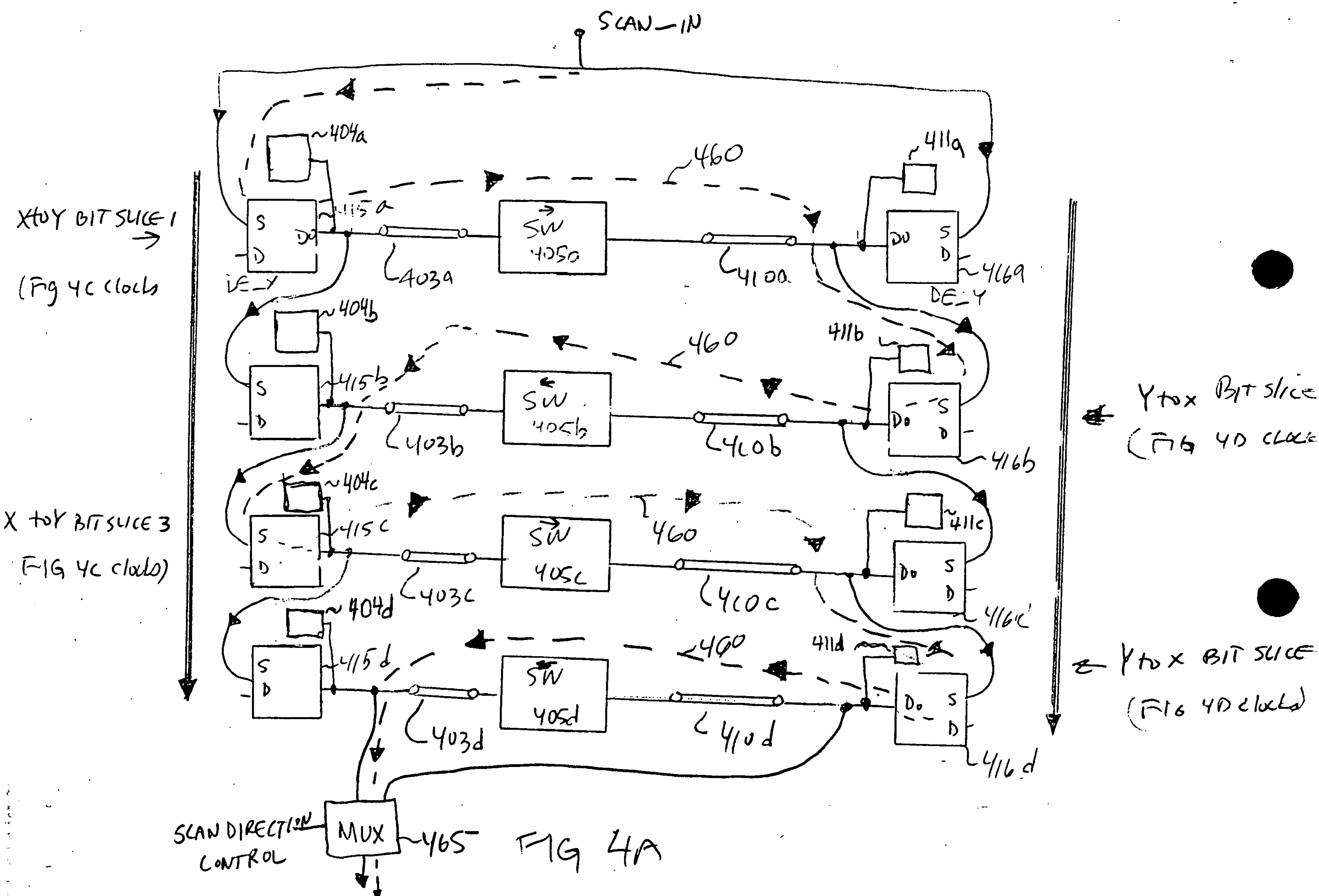

SCAN_IN
X to Y BIT SLICE 1
(FIG 4C clock
X to Y BIT SLICE 3
FIG 4C clock)
Y to X BIT SLICE
(FIG 4D clock
Y to X BIT SLICE
(FIG 4D clock)
404a
404b
404c
404d
415a
415b
415c
415d
403a
403b
403c
403d
SW
405a
SW
405b
SW
405c
SW
405d
410a
410b
410c
410d
411a
411b
411c
411d
416a
416b
416c
416d
460
460
460
460
DE_Y
DE_Y
MUX
465
SCAN DIRECTION
CONTROL

FIG 4A

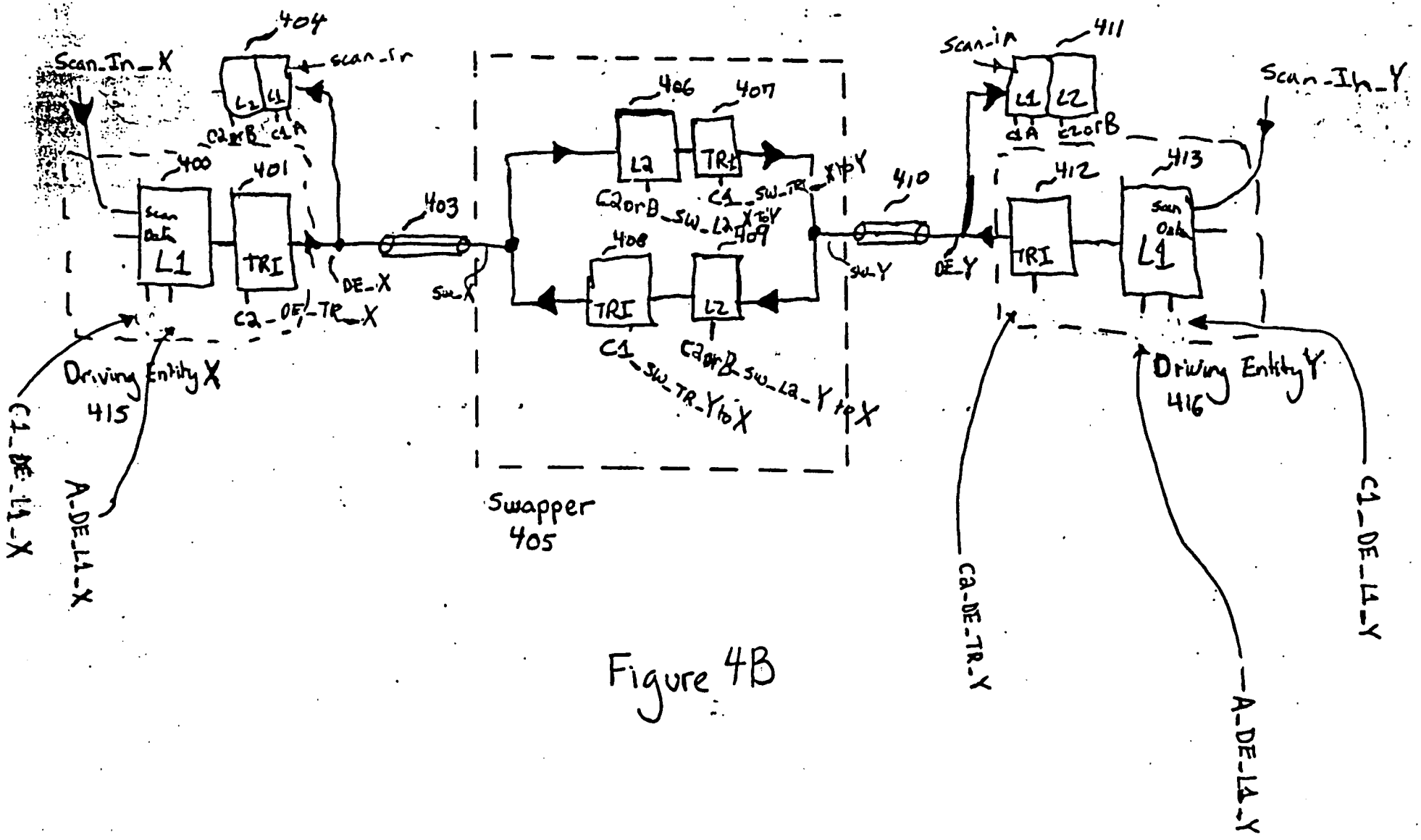
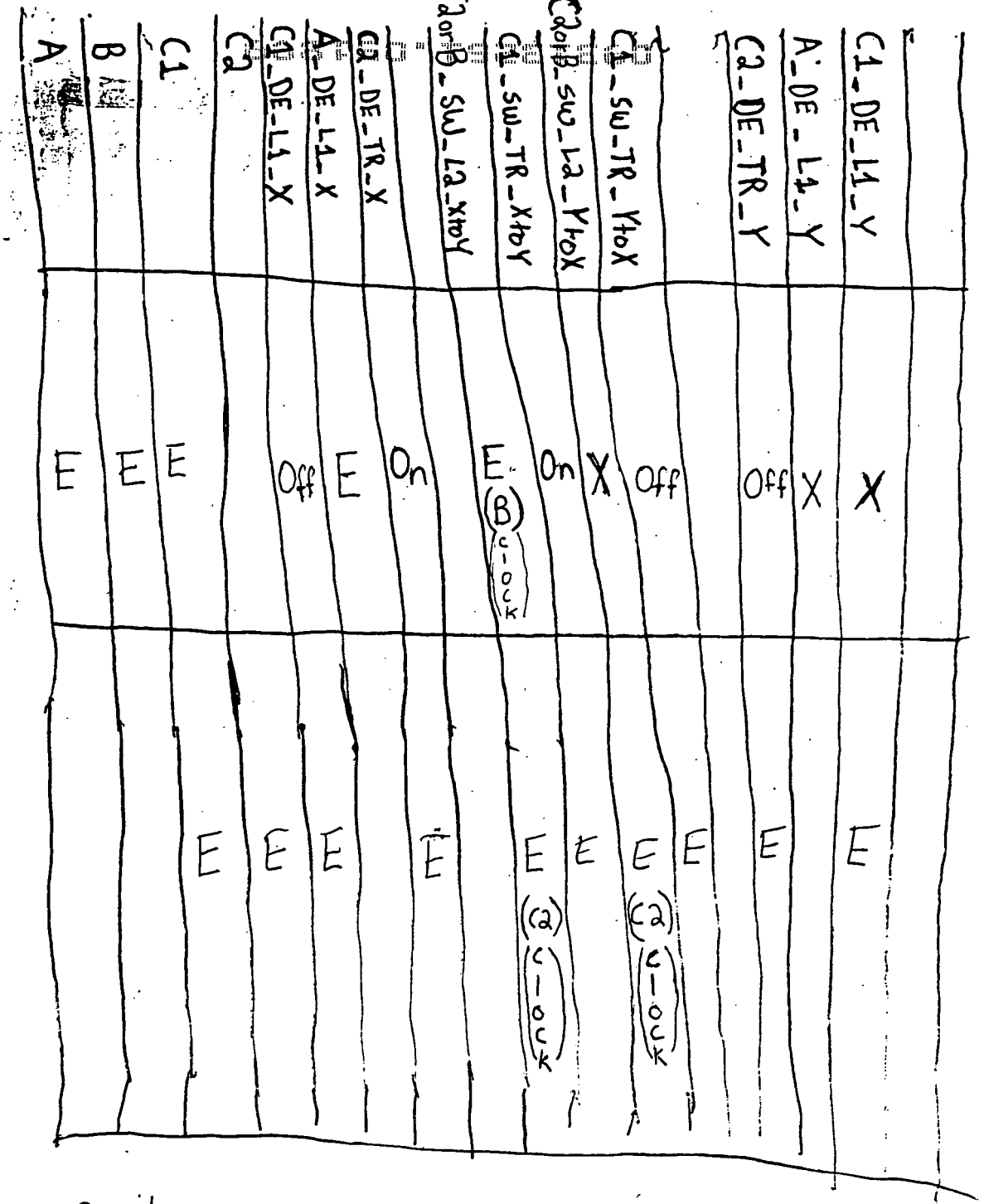


Figure 4B



Clocks for XtoY ~~B/X Shift~~ transfer

Figure 4C

	Combined Scan and Test Modes	System Mode
C1_DE_L1_Y	Off	E
A_DE_L1_Y	E	E
C2_DE_TR_Y	On	
		E
C1_SW_TR_YtoX	On	E (C2 clock)
C2orB_SW_L2_YtoX	E (B clock)	E
C1_SW_TR_XtoY	Off	E (C2 clock)
C2orB_SW_L2_XtoY	X	
		E
C2_DE_TR_X	Off	
A_DE_L1_X	X	E
C1_DE_L1_X	X	E
C2		E
C1	E	
B	E	
A	E	

Clocks for XtoY ~~Bypass~~ transfer

Figure 4D

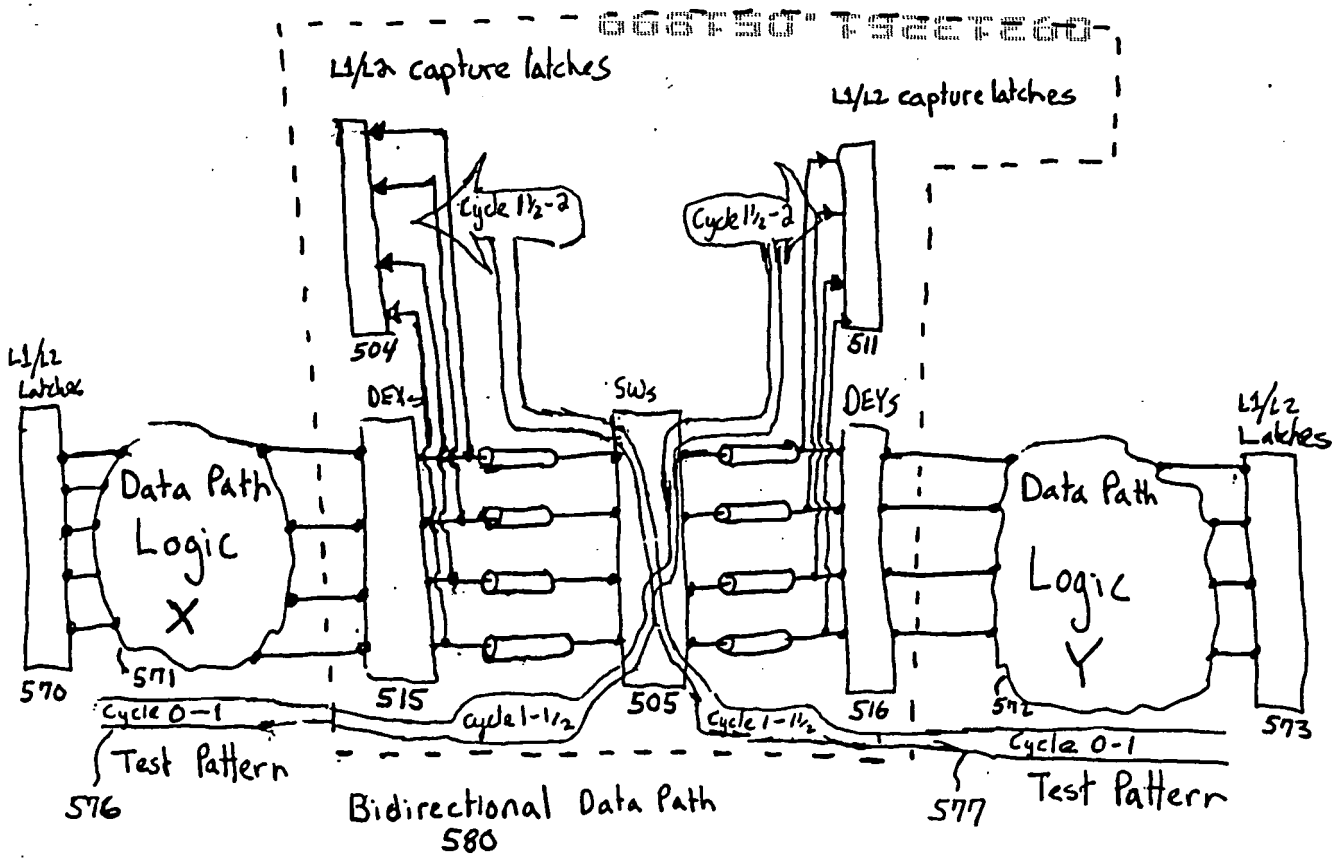
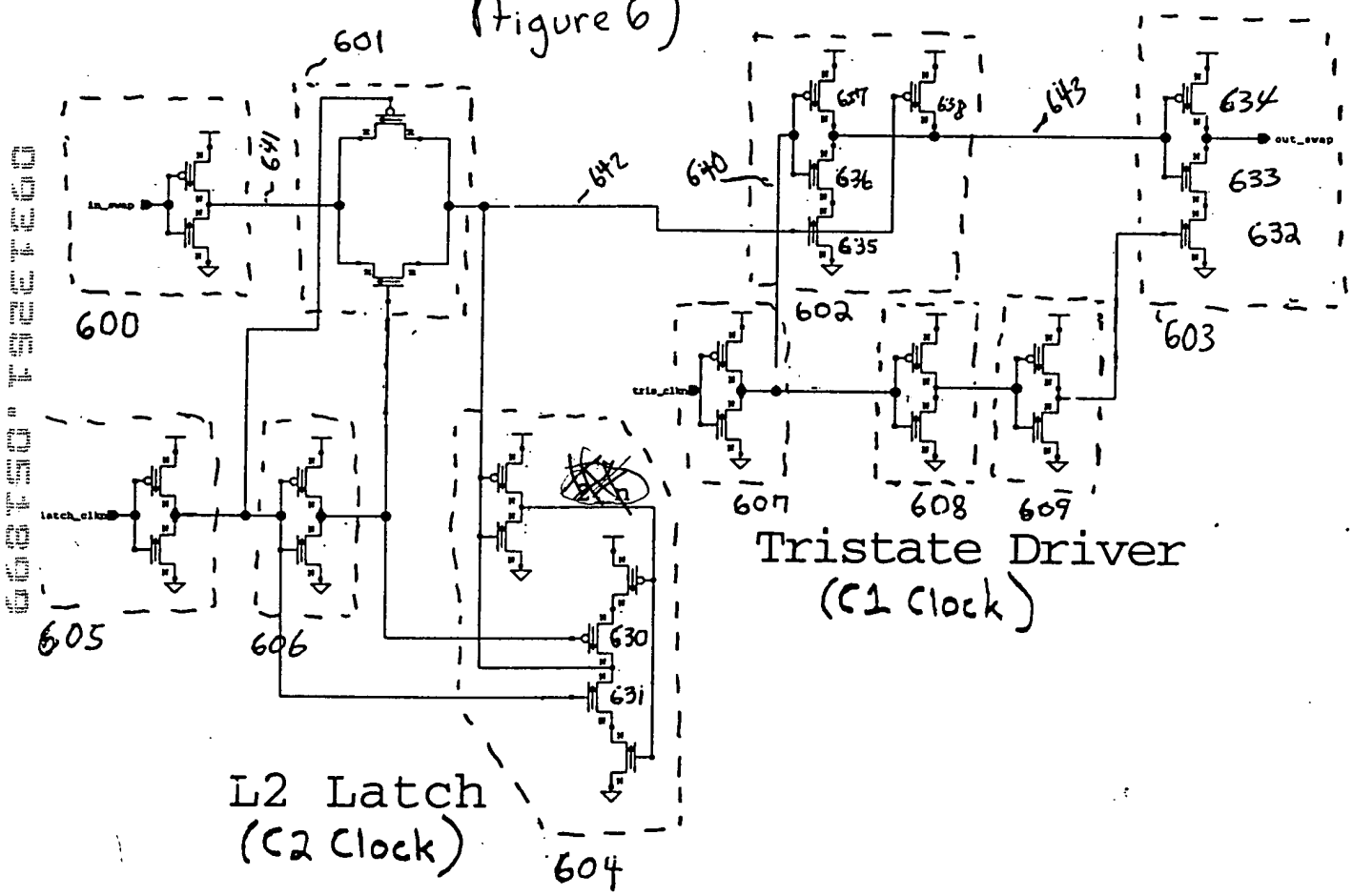
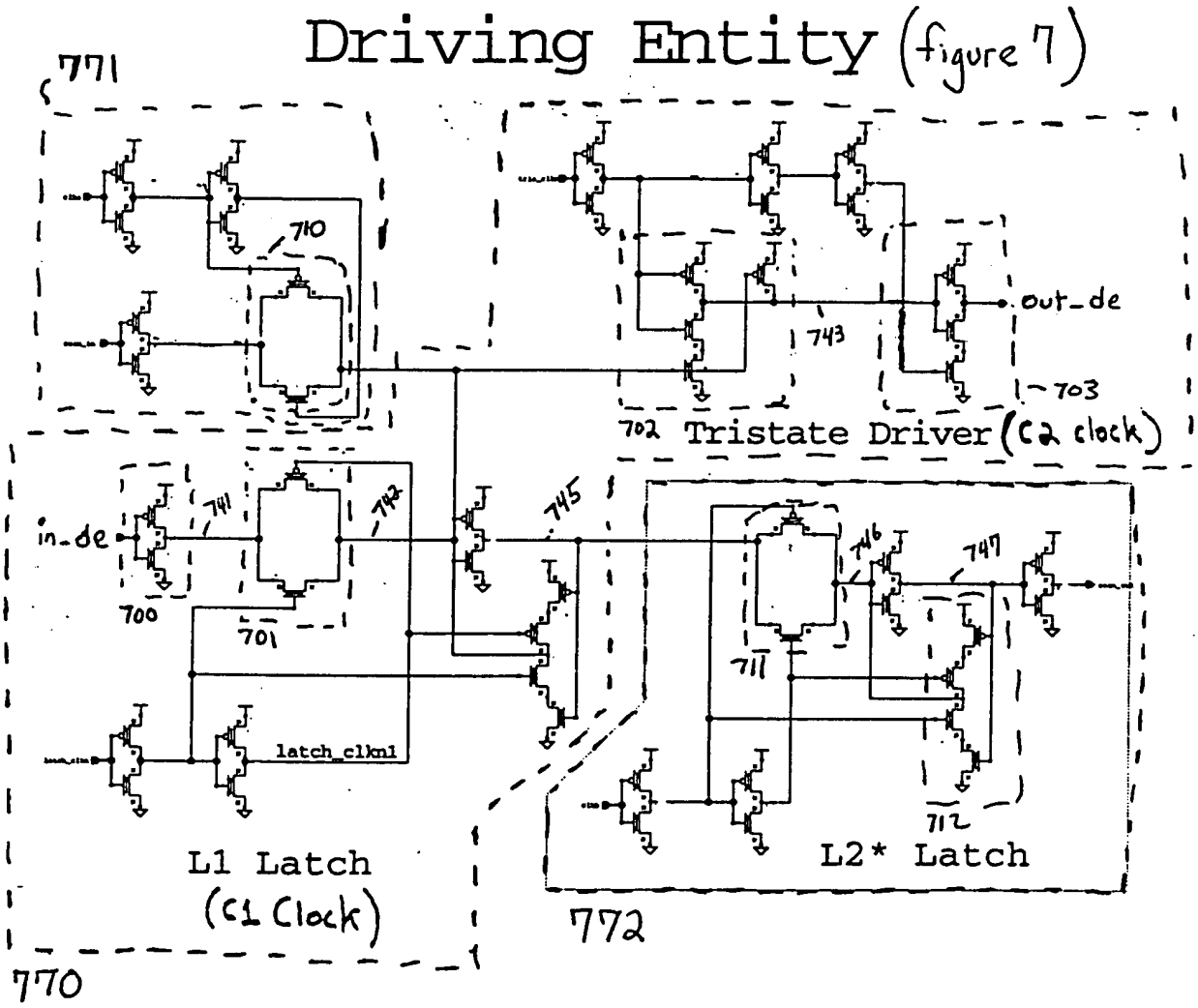

L1/L2 capture latches
L1/L2 capture latches
Cycle 1½-2
Cycle 1½-2
504
511
L1/L2 Latches
DEX
SWS
DEYS
L1/L2 Latches
Data Path Logic X
Data Path Logic Y
570
571
515
505
516
572
573
Cycle 0-1
Cycle 1-1½
Cycle 1-1½
Cycle 0-1
Test Pattern
Test Pattern
576
Bidirectional Data Path
580
577

Figure 5

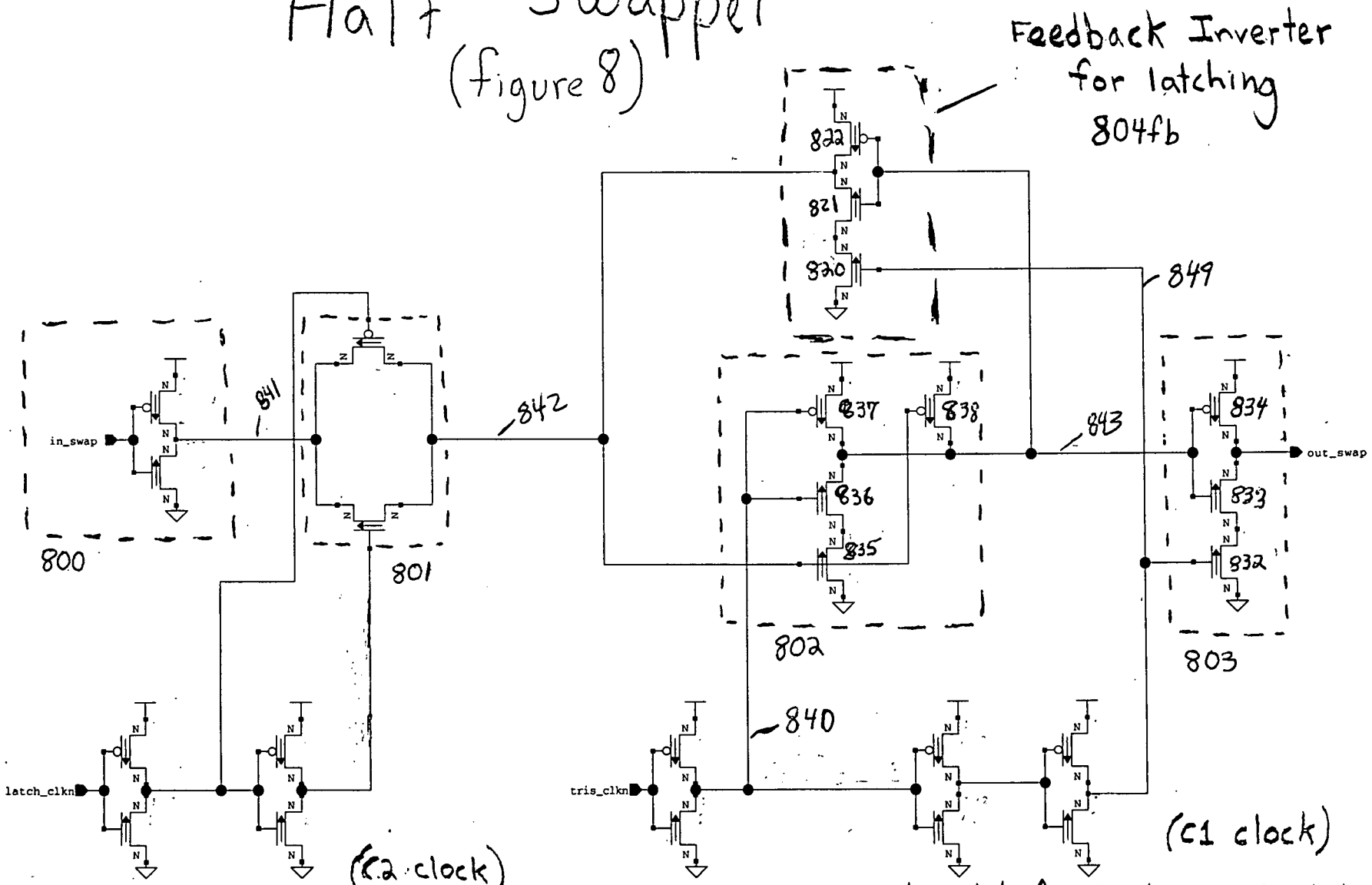
Half Swapper

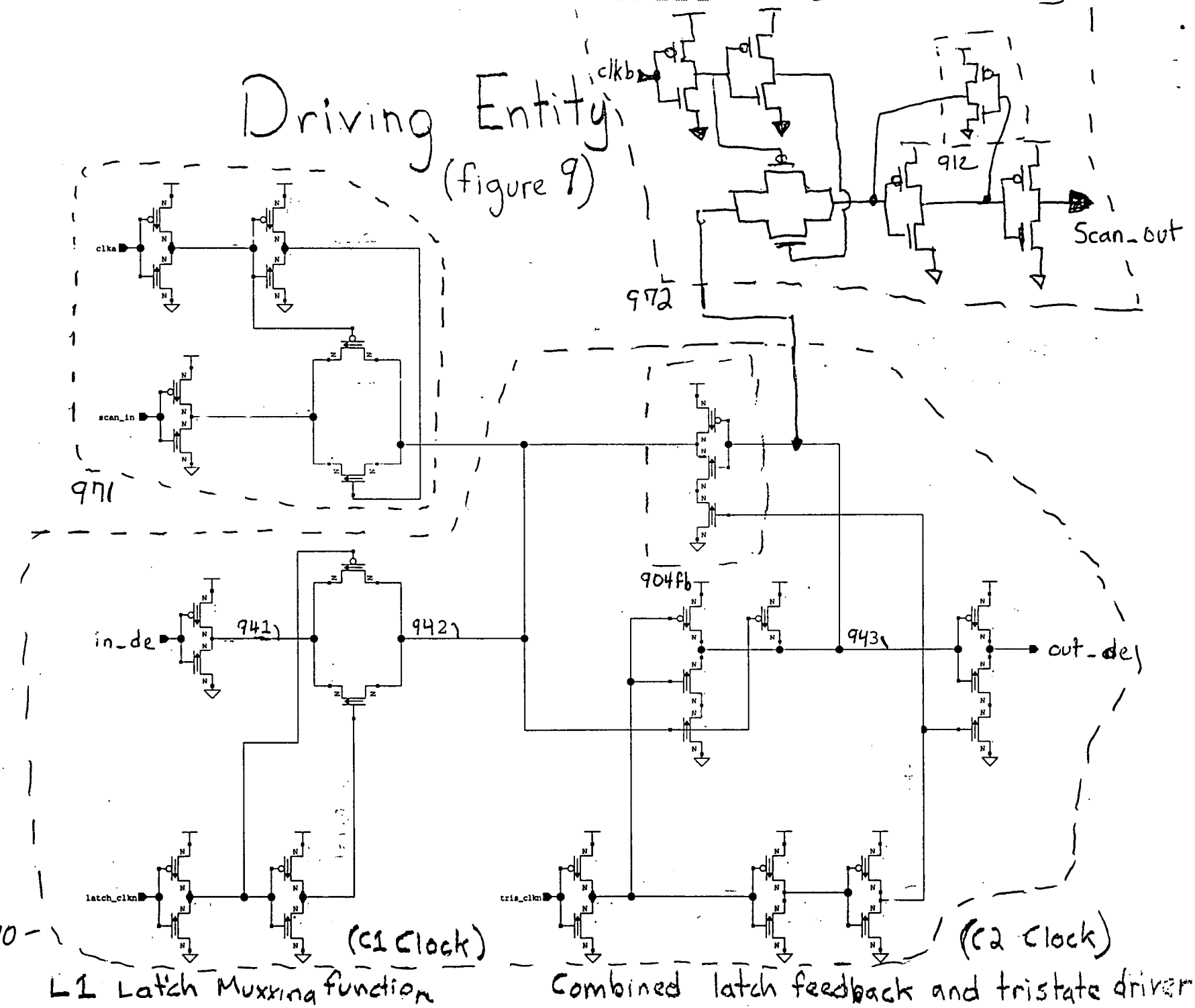
(figure 6)



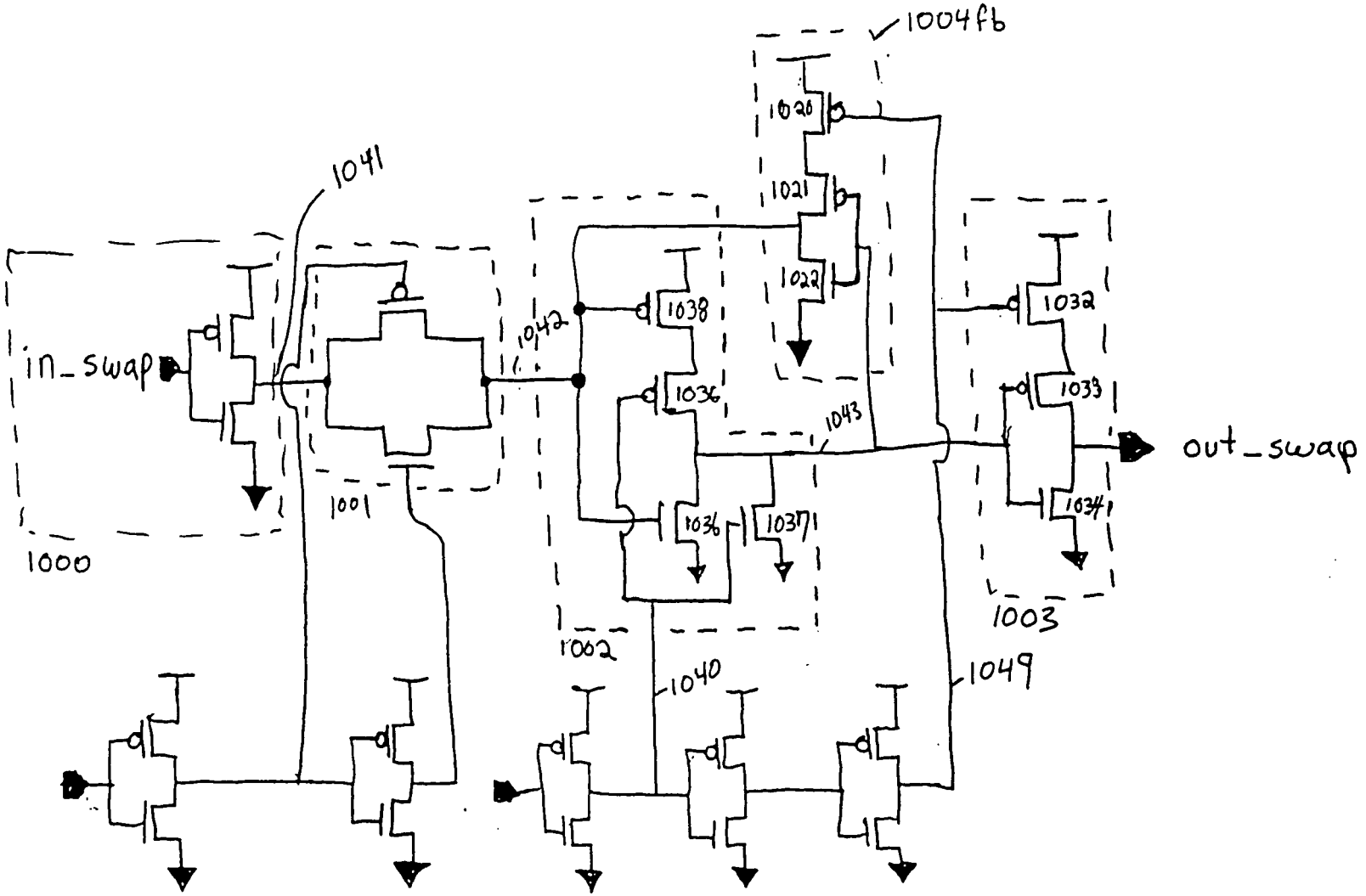

Driving Entity (figure 7)
771
710
out_de
743
703
702 Tristate Driver (C2 clock)
in_de
741
742
745
700
701
latch_clkn1
746
747
711
712
L1 Latch
(C1 Clock)
L2* Latch
772
770

Half Swapper (figure 8)





Half Swapper (figure 10)



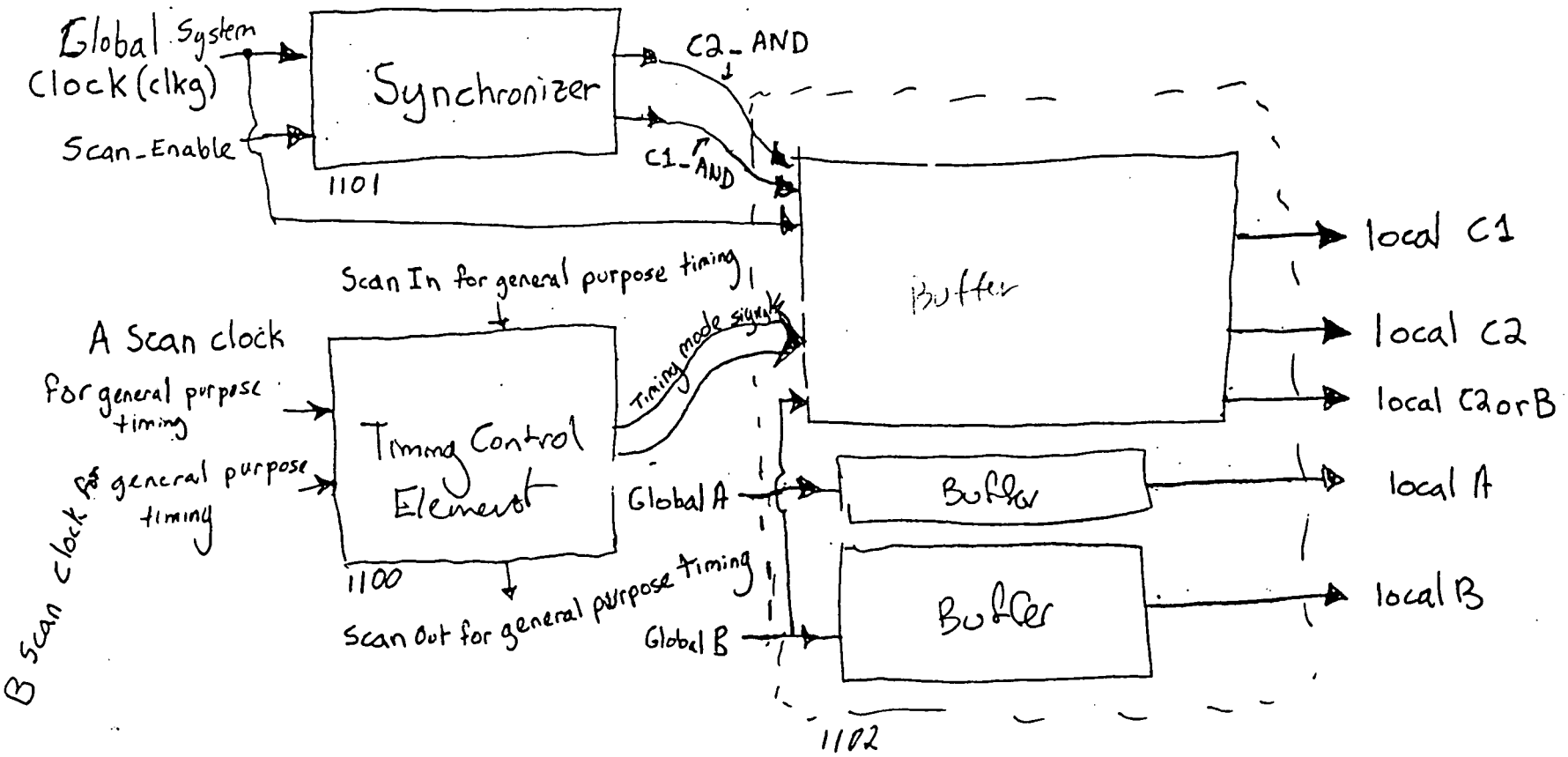

Global System Clock (clkg)
Scan_Enable
Synchronizer
1101
C2_AND
C1_AND
Buffer
local C1
local C2
local C2orB
Scan In for general purpose timing
A Scan clock for general purpose timing
B scan clock for general purpose timing
Timing Control Element
1100
Timing mode signal
Global A
Global B
Scan Out for general purpose timing
Buffer
Buffer
local A
local B
1102

Figure 11

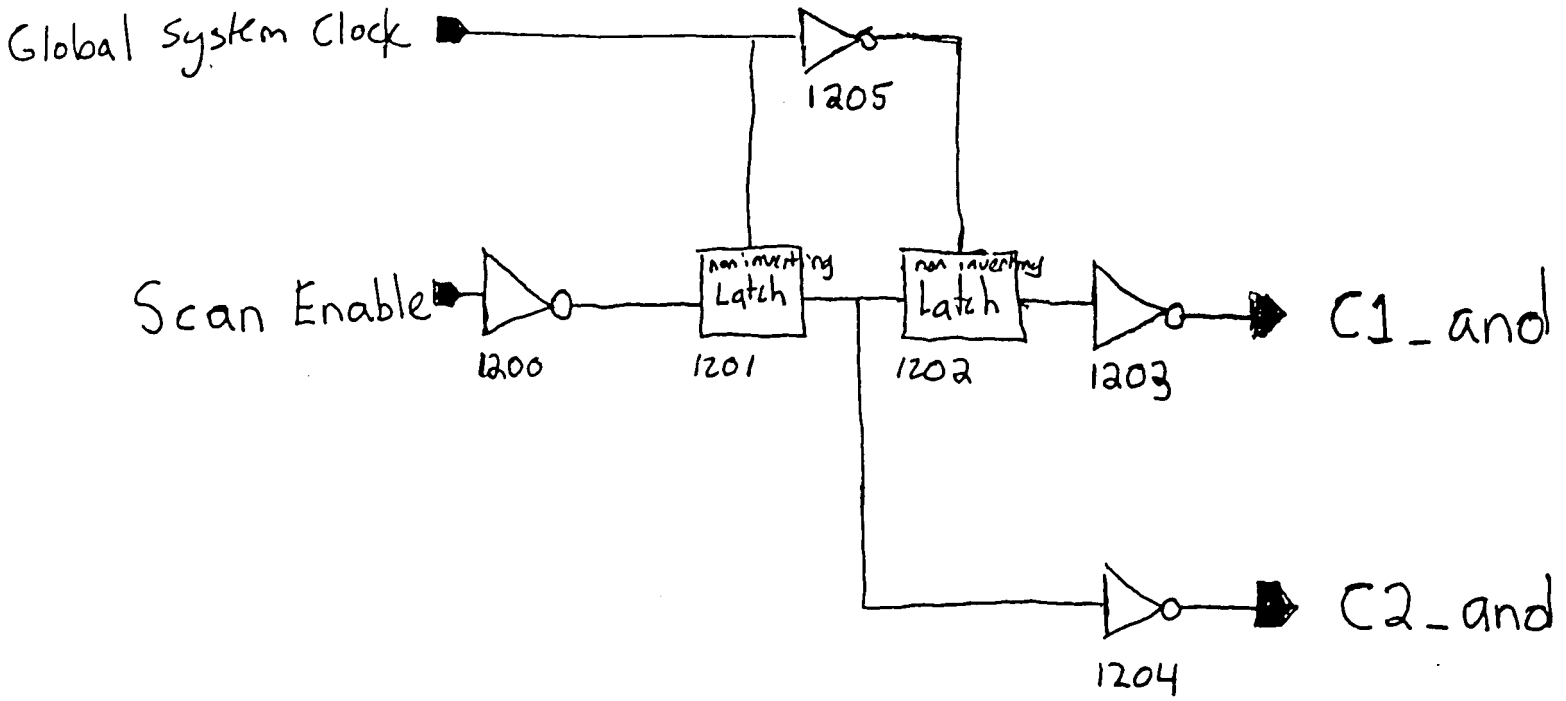


Figure 12

Figure 13

System Clocks for the Driving Entities

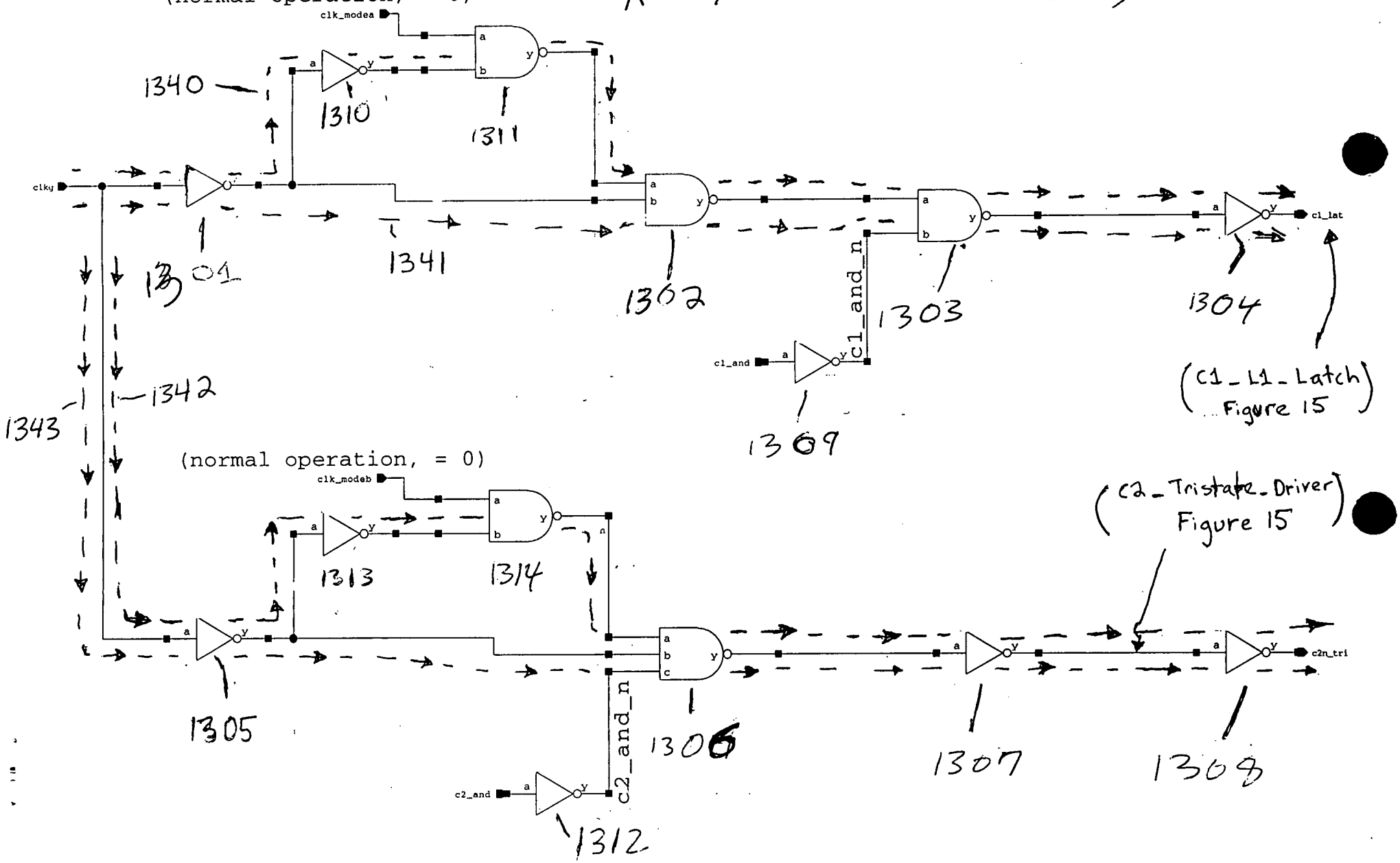


Figure 14

Clocks for the full Swappers

(approx. power level = 32 full swappers)

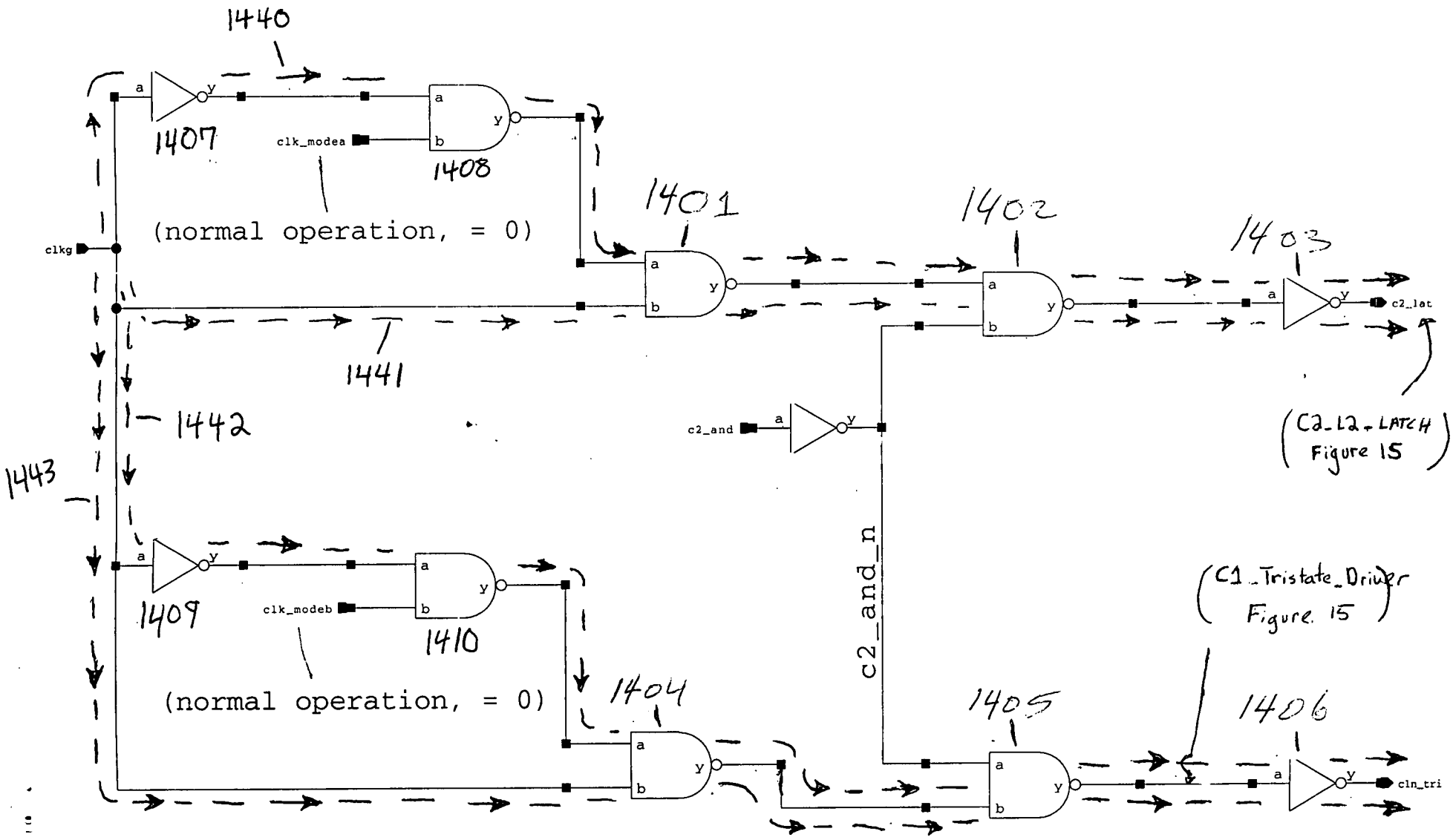


Figure 15

The above understood and witnessed by

Date

and by

Date